CLAIM AMENDMENTS

Please amend the claims by canceling claims 1 – 6, 22 – 27 and 52, without prejudice, and replace them with new claims 64 – 70, as indicated on the following listing of all the claims in the present application after this Amendment:

1 – 63. (cancelled)

64. (new) Flash memory formed on an integrated circuit substrate, comprising:

a plurality of global bit lines,

a plurality of global control lines,

a plurality of memory cell array segments that individually comprise

a plurality of source and drain diffusions elongated in a first direction across the substrate and being spaced apart in a second direction, the first and second directions being perpendicular with each other,

a two-dimensional array of charge storage elements with at least one charge storage element being coupled with at least a portion of individual memory cell channels formed between adjacent source and drain diffusions in the second direction,

a plurality of control lines with lengths extending across the charge storage elements in the first direction forming control gates operably coupled therewith and being spaced apart in the second direction,

a first plurality of select transistors connected between the plurality of source and drain diffusions and the plurality of global bit lines, and

a second plurality of select transistors connected between the plurality of control lines and the plurality of global control lines,

whereby the individual memory cell array segments may be selectively connected with the global bit and control lines by activating their respective first and second plurality of select transistors.

65. (new) The memory of claim 64, wherein the plurality of memory cell array segments additionally individually comprise a plurality of word lines with lengths extending in

the second direction over the control lines and coupled with a portion of individual memory cell channels adjacent their at least one charge storage element, the plurality of word lines being spaced apart in the first direction.

66. (new) The memory of claim 65, wherein the plurality of word lines are additionally coupled with their said adjacent charge storage elements in a manner to erase charge from said charge storage elements.

67. (new) The memory of claim 65, wherein the array of charge storage elements includes two charge storage elements coupled with portions of the individual memory cell channels adjacent the source and drain diffusions, and the portion of the channels to which the word lines are coupled is positioned between the two charge storage elements.

68. (new) The memory of claim 64, wherein the plurality of global bit lines and the plurality of global control lines are made of a metal.

69. (new) The memory of any one of claims 64 – 68, wherein the charge storage elements are conductive floating gates.

70. (new) The memory of any one of claims 64 – 68, wherein the charge storage elements are operated to store more than two levels of charge thereon, thereby to store more than one bit of data per charge storage element.